The Relevance of TCAD to Process-Aware Design

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Summary

- Two approaches to reduce device size and process variation

  1. Improve each process module, and tightly integrate modules
  2. Learn to live with (or accommodate) intrinsic process variation, and exploit these in design

- Need physical models of the different phenomena that govern process variation, integrated in a suitable framework – TCAD provides such a framework
- Will describe the general TCAD framework, as it exists at Intel, and give some specific examples of design-process interactions

Outline

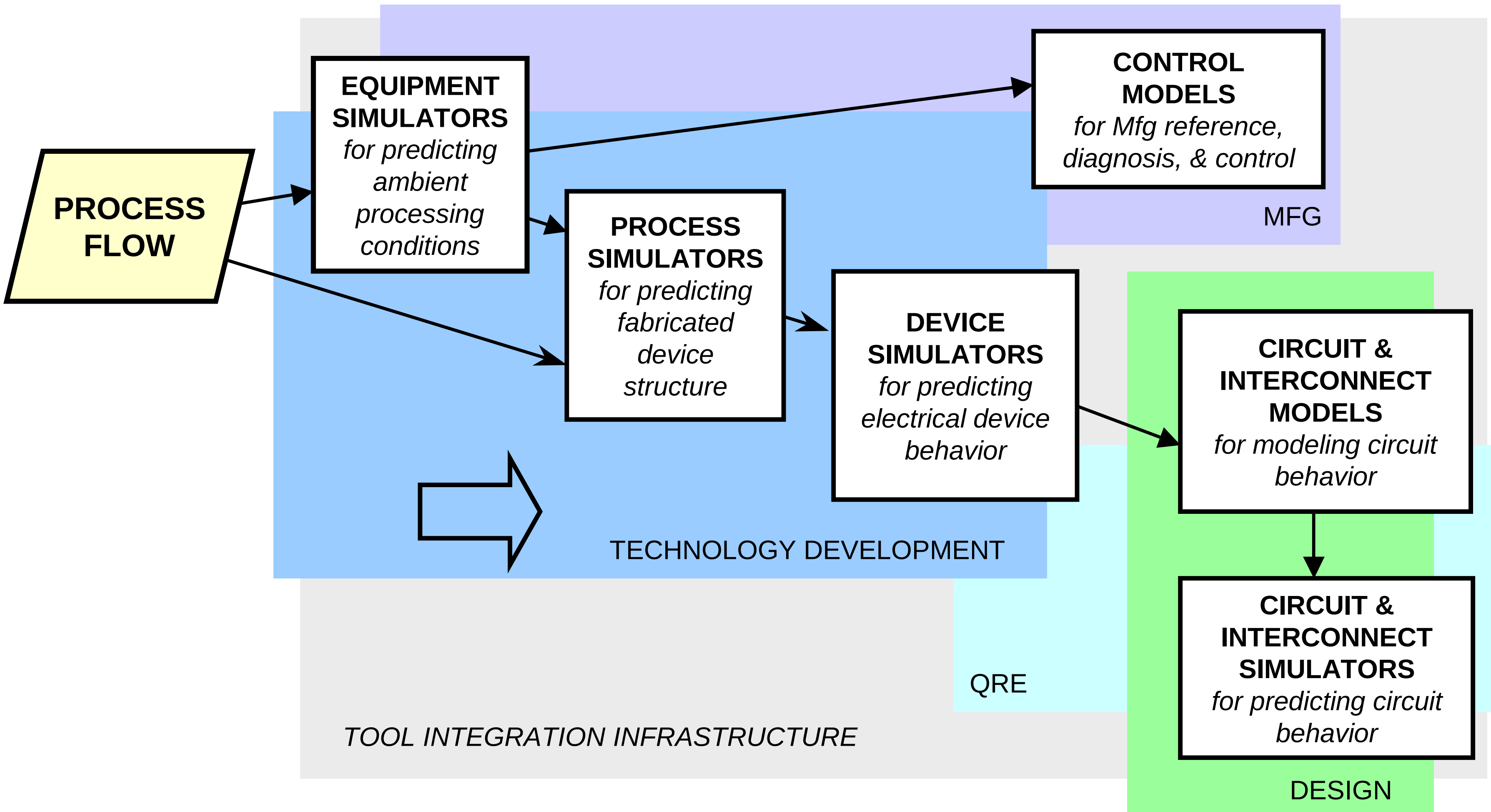
- Relationship of TCAD with technology development
- TCAD infrastructure
- Focus on aspects of Lithography – Design coupling
  - Some challenges in OPC
  - Impact of aberrations on design
  - Layout dependent flare in EUV
  - Litho/CMP/Design interactions
- Future Directions

Technology Cycle: a driver for TCAD

	Plannning/Research			Development			Manufacturing		
Year	-6	-5	-4	-3	-2	-1	1	2	3

	Plannning/Research	Development	Manufacturing
$/Year	~ 10^7	~ 10^8	~ 10^9
Risk	High	Moderate	Low
Technical Focus	Evaluate	Integrate	Control
Modeling Focus	Explore	Optimize	Control

TCAD Tool Categories



COMMON CHARACTERISTIC: PROCESS-DEPENDENT MODELING

The necessary expertise…

Scientific Disciplines	Areas of Expertise	Simulators
Electrical Eng.	Circuit Design	Circuit Reliability
Physics	Layout Design	Circuit
Applied Math.	Device Physics	Package
Material Science	Reliability	Plasma Etch/Dep
Mechanical Eng.	Plasma Physics	Topography
Chemical Eng.	Control Theory	CMP
Computer Science	Optimization	Lithography
	Statistical Analysis	Device
	Numerical Meth.	Bulk Si
	Grid - Solid Mod.	Electrodeposition
	Diffusion Theory	RTP
	Surface Chemistry	Interconnect
	Thermal/Stress	Die LevelThermal
	Graphics/Visualiza.	
	SW Design	
	Mass Transport	

Reusable Component Library

Capability
2D/3D Visualization
Statistical Analysis
DOE Generation
Optimization API
Job Control (UNIX/NT)
Electrical Data Extraction
Solid Modeler
Bitmap Image Viewer
Layout reader/writer
Layout Editor
Geometric Parameterization
Graphical Structure Editor
Layout Sizing
Parameter Extraction
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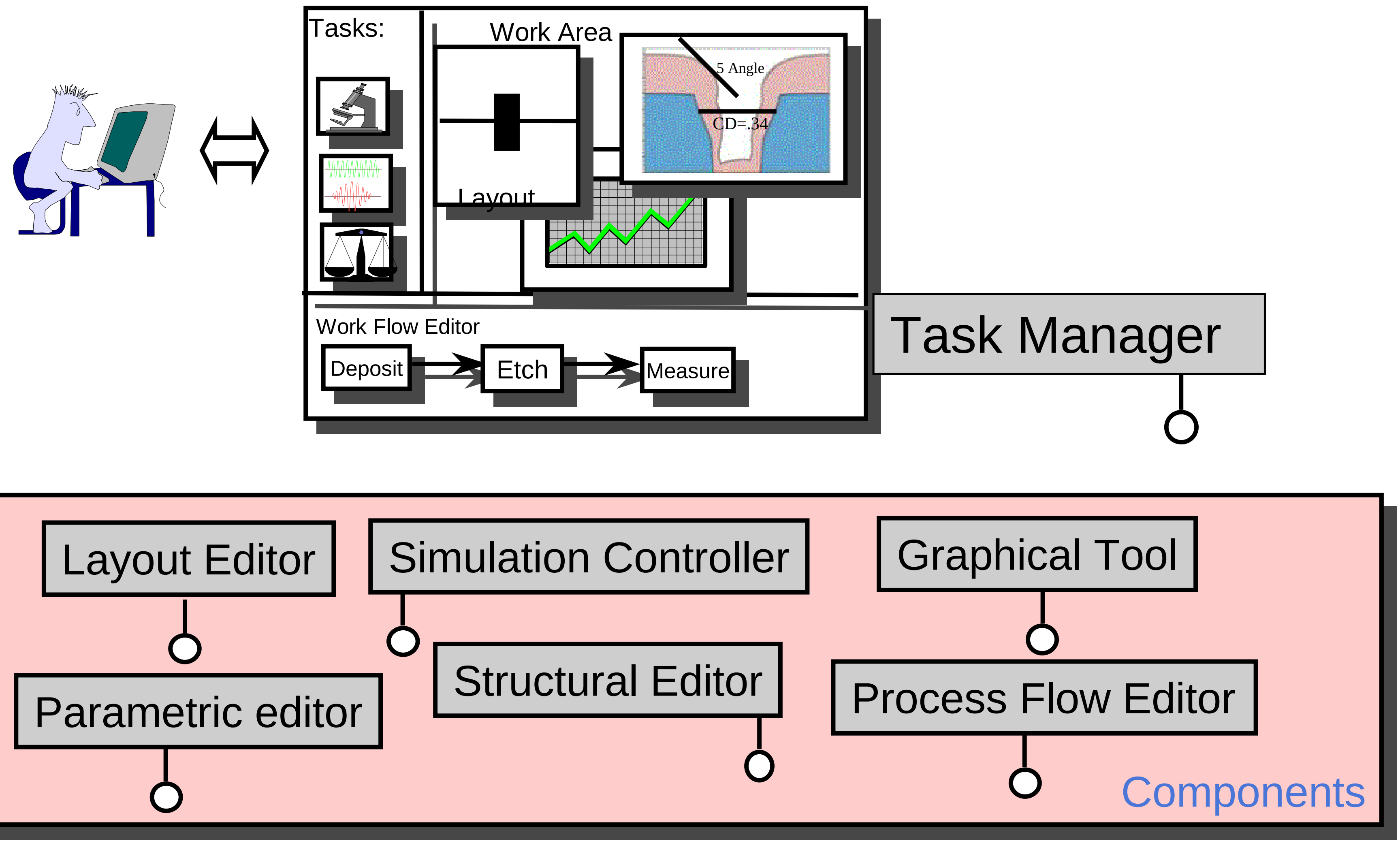
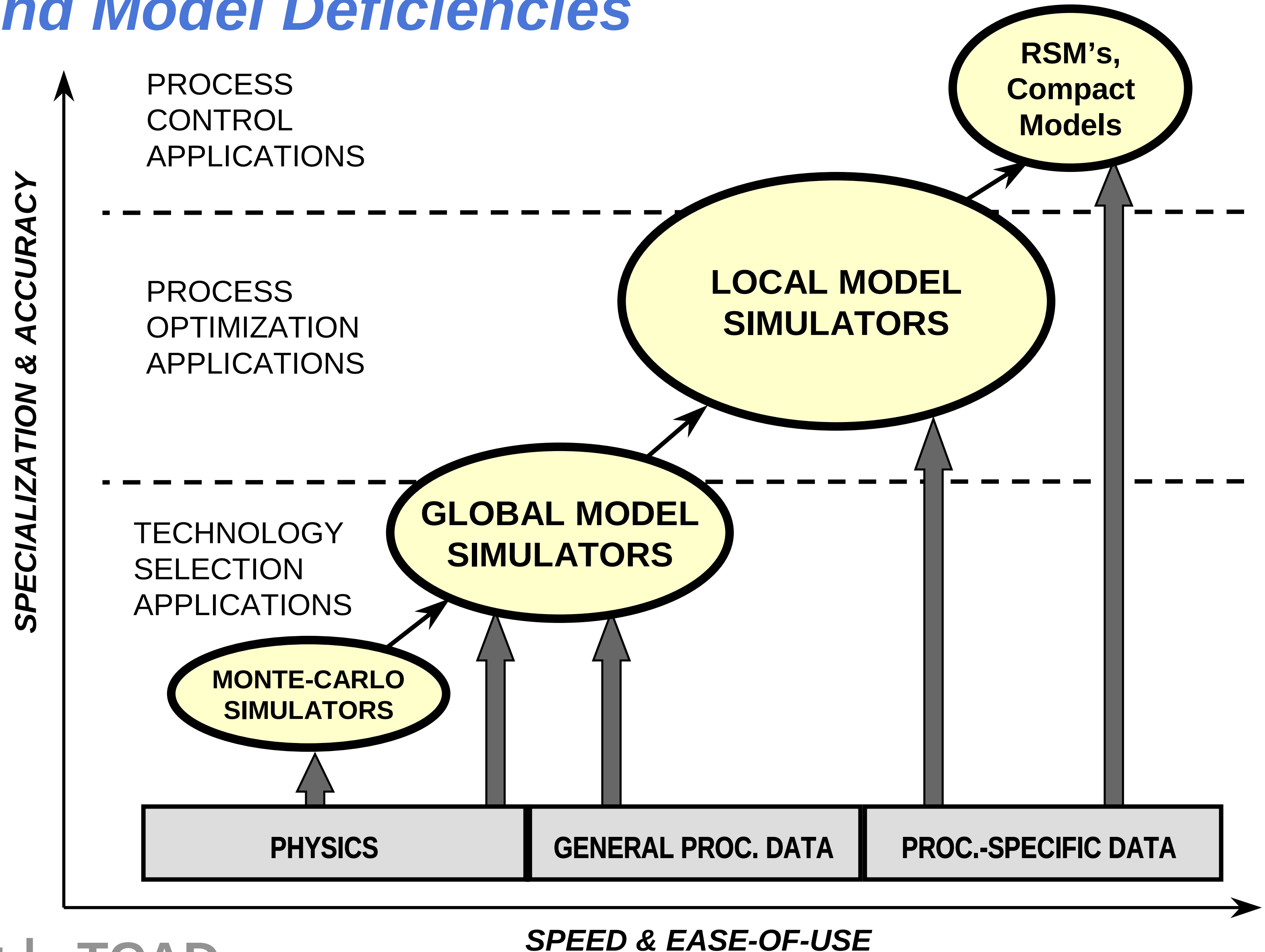
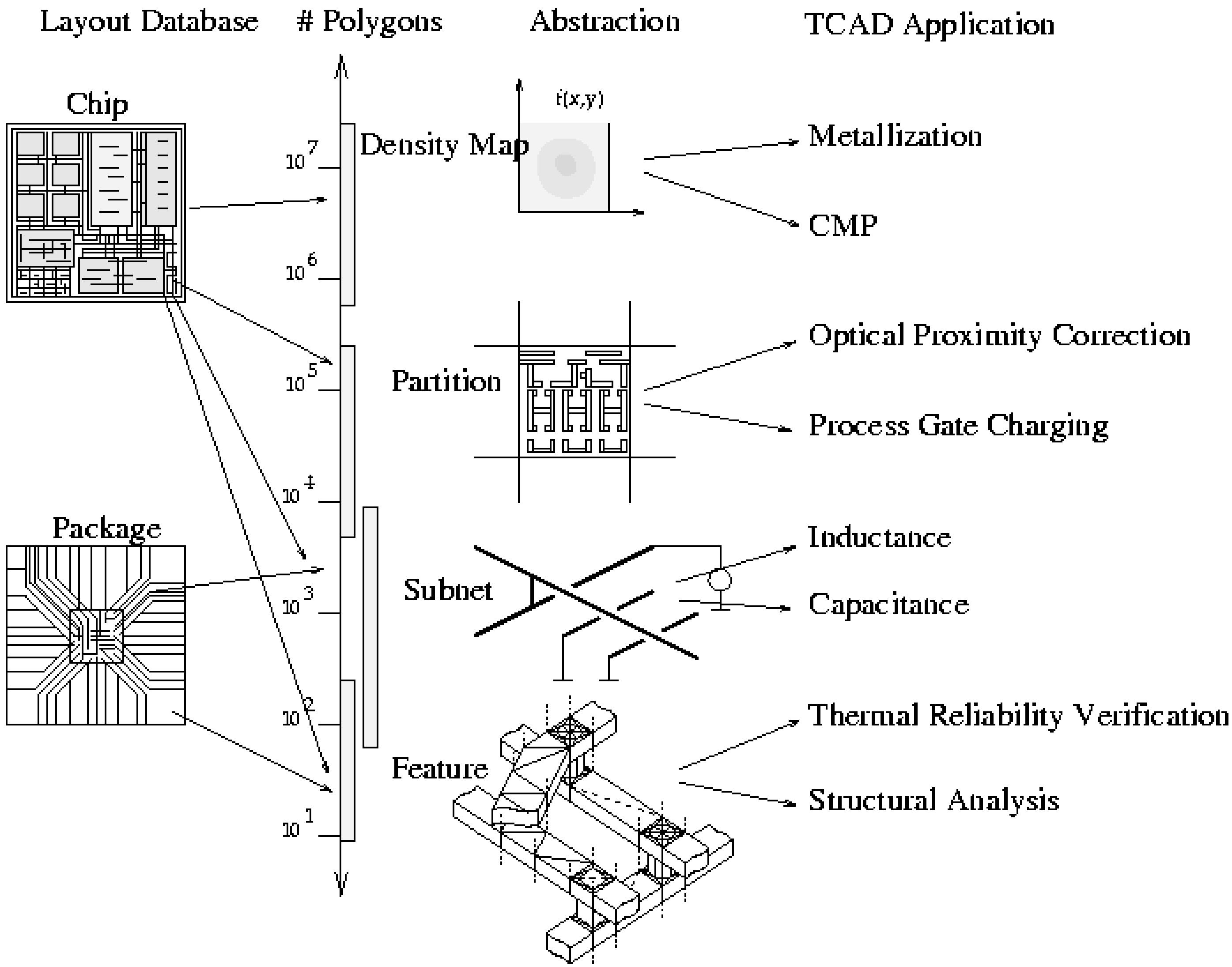
Interactive Applications - Architecture



Model Hierarchies Allow Us to Address Speed and Model Deficiencies



Layout info increasingly critical in TCAD



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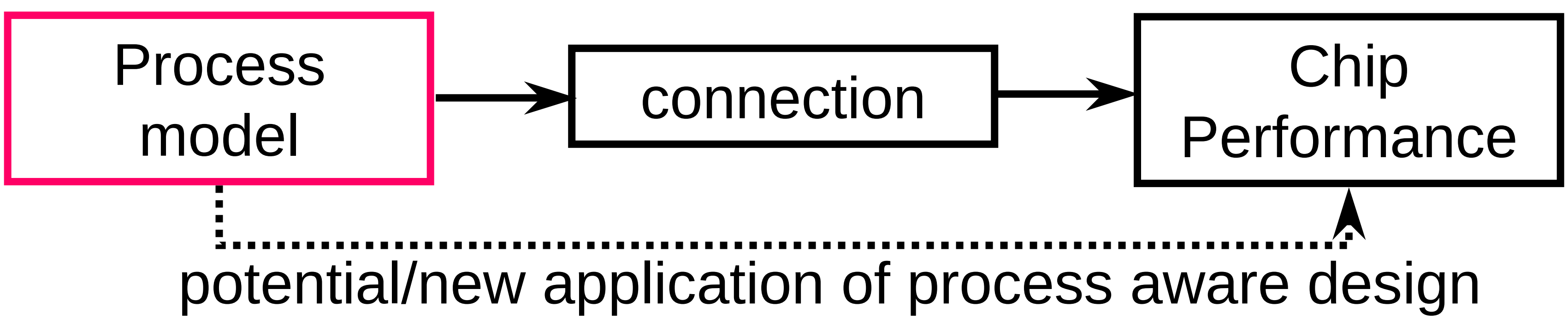
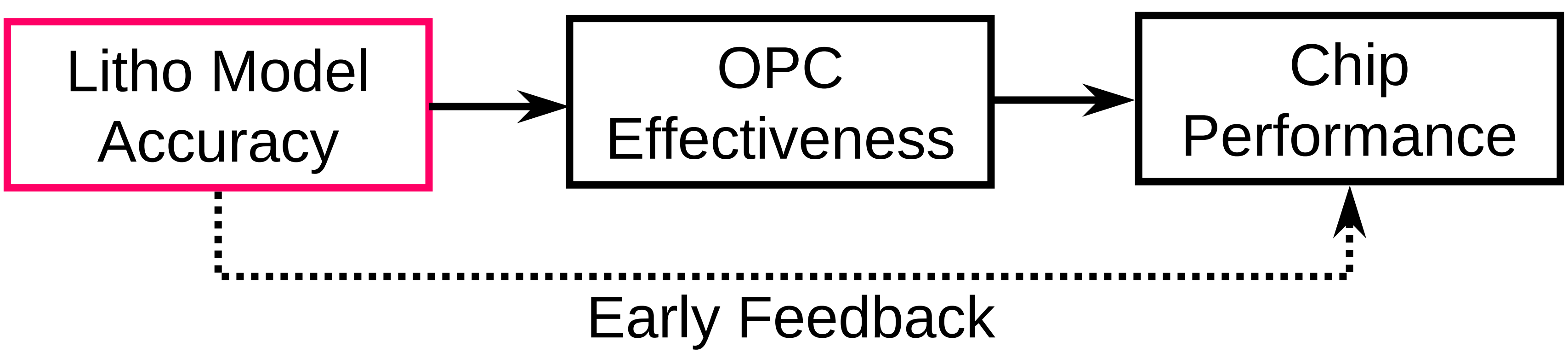
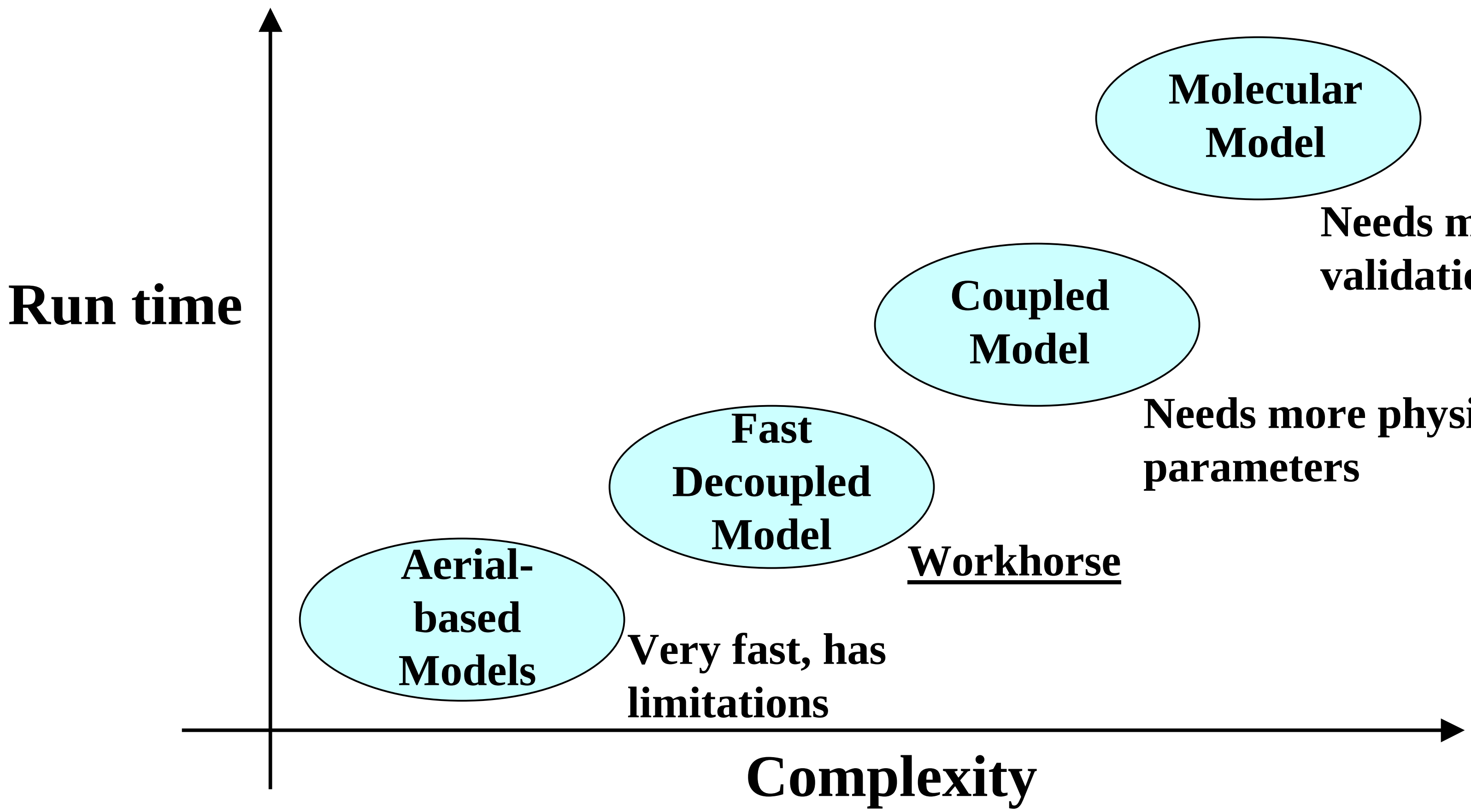


Example 1: modeling hierarchy for OPC

- Today, OPC is one of the most active interfaces between process and design
- The accuracy of lithography models is a critical enabler for OPC
- Accurate lithography model development faces many challenges – an excellent illustration of need for hierarchical model development



Hierarchy of resist models



Typical Resist Modules

- Exposure/Bleaching (Dill Model)

$$\frac{dI}{dz} = -\alpha I \qquad \alpha = AM + B \qquad \frac{dM}{dt} = -CIM$$

- PEB (Coupled Reaction Diffusion)

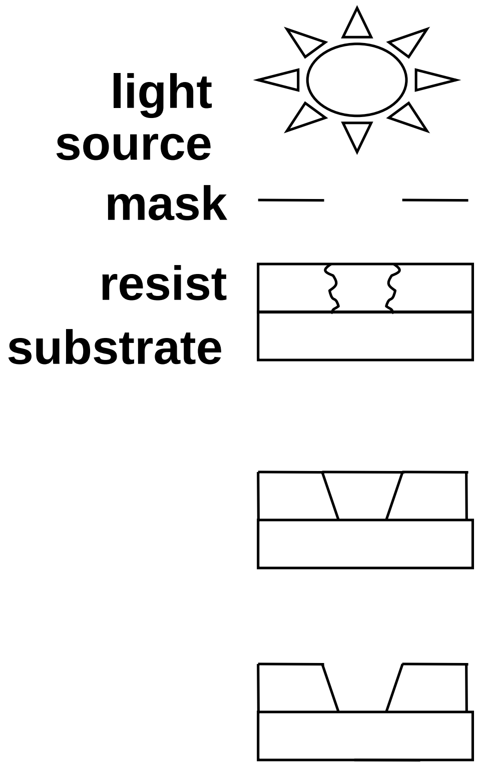
$$\frac{\partial [M]}{\partial t} = -K_{amp} [M][H]^{m}$$

$$\frac{\partial [H]}{\partial t} = \frac{\partial}{\partial x}\left(D_{H} \frac{\partial [H]}{\partial x} \right)$$

- Development (Mack Model)

$$R = R_{max} \frac{(\alpha+1)(1-M)^{n}}{\alpha+(1-M)^{n}} + R_{min} \qquad \alpha = \frac{(n+1)}{(n-1)}(1-m_{th})^{n}$$

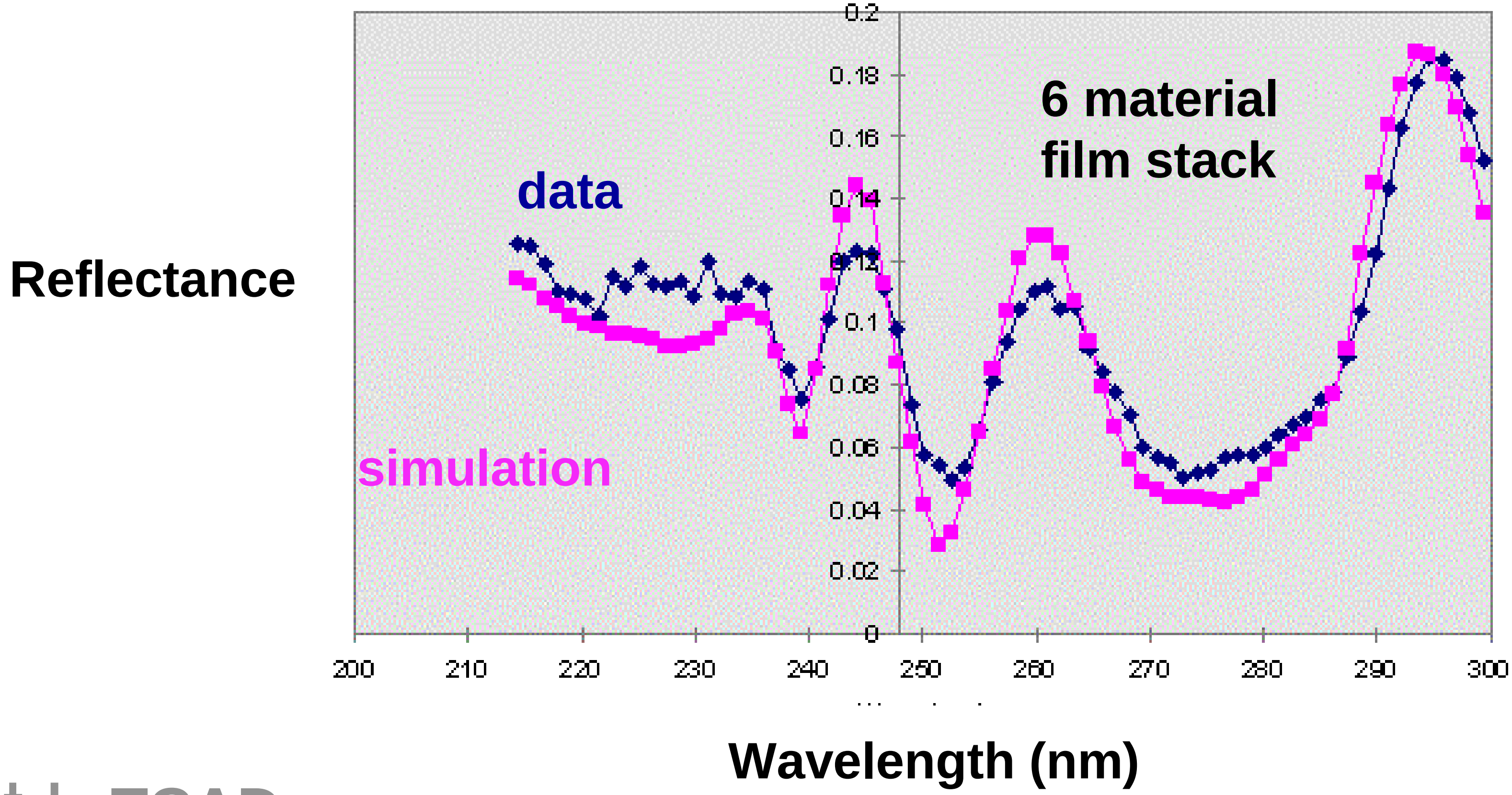
Experimental Measurements



Litho Module	Parameters	Measurement
Exposure	**n, A, B, C**	**n&k Analyzer**
Bake	**K_{amp}, D, m**	**FTIR**
Development	**Rmax, Rmin, mth, n**	**DRM**

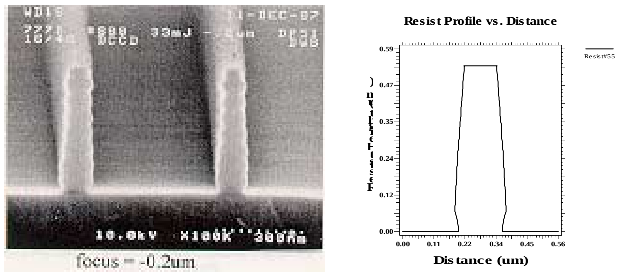
Measuring actual films is important

- Film refractive index strongly depends on processing conditions
- Comparison of measured and simulated reflectance

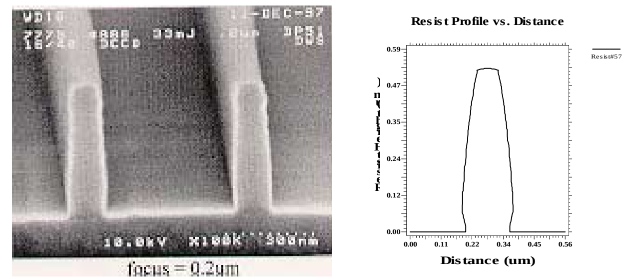


intel® TCAD

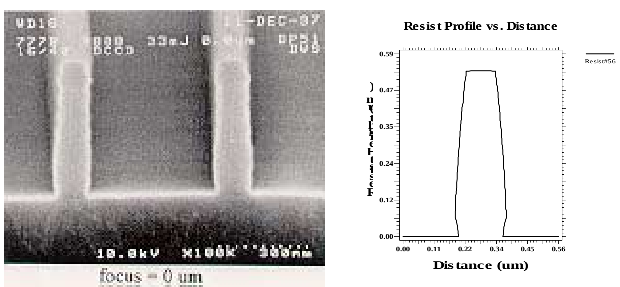
Match 1) resist profiles,
2) through focus data….



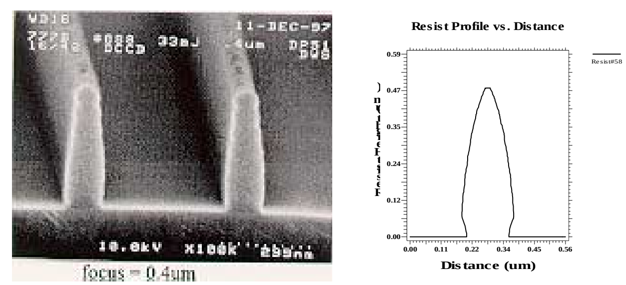
-0.2 µm defocus



0.2 µm defocus

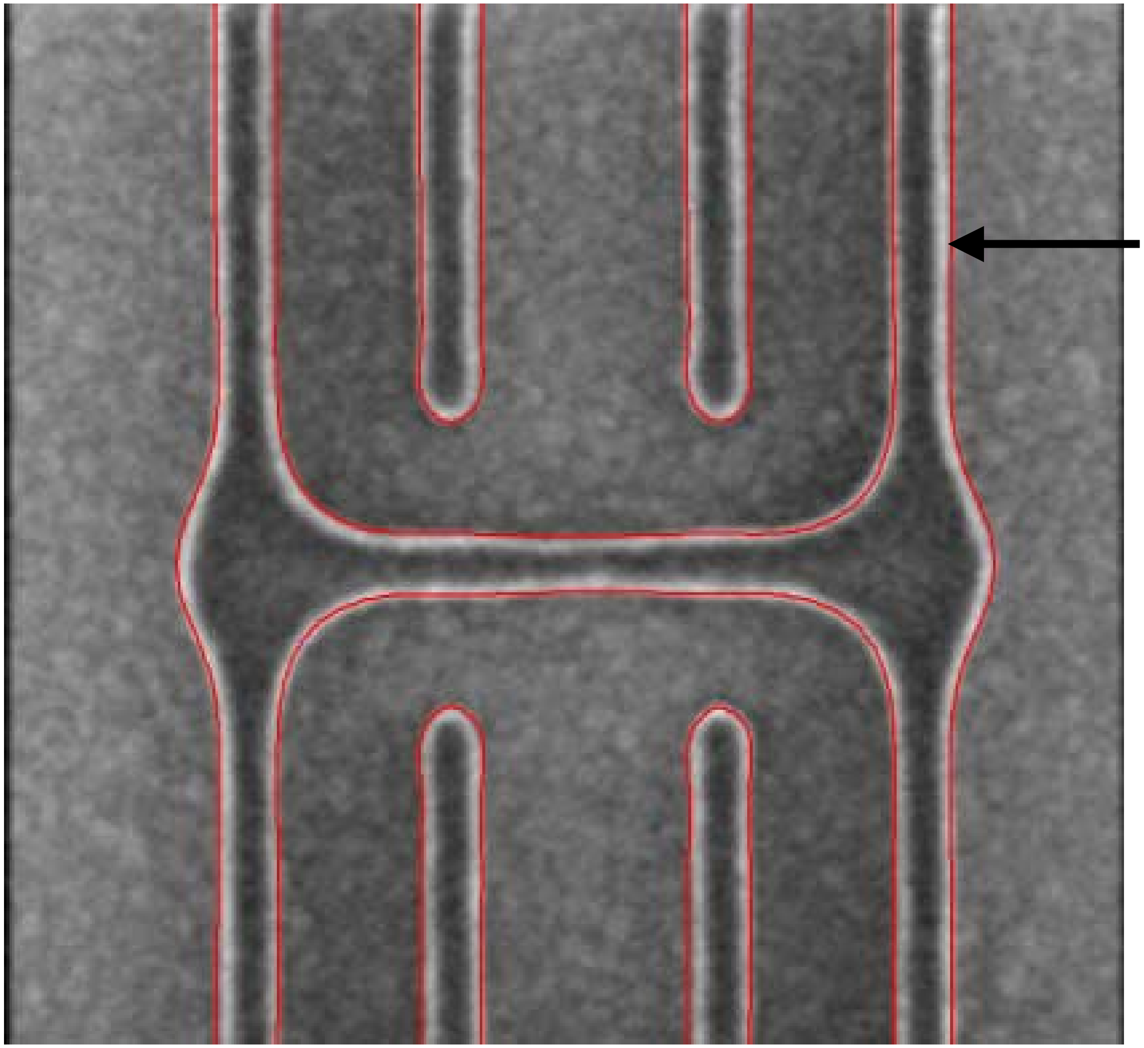


0 µm defocus



0.4 µm defocus

….as well as 3) 2D structures



simulation

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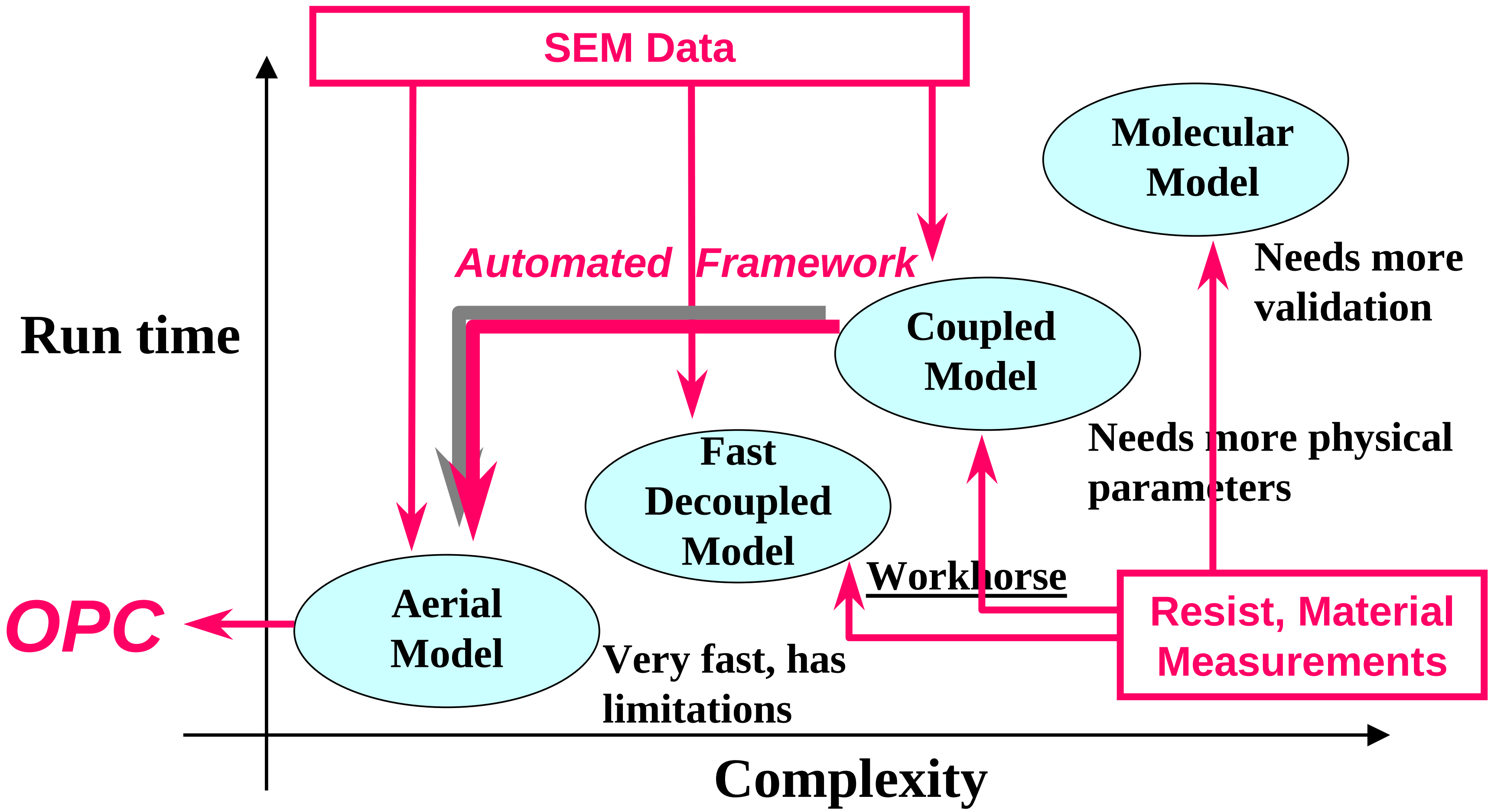
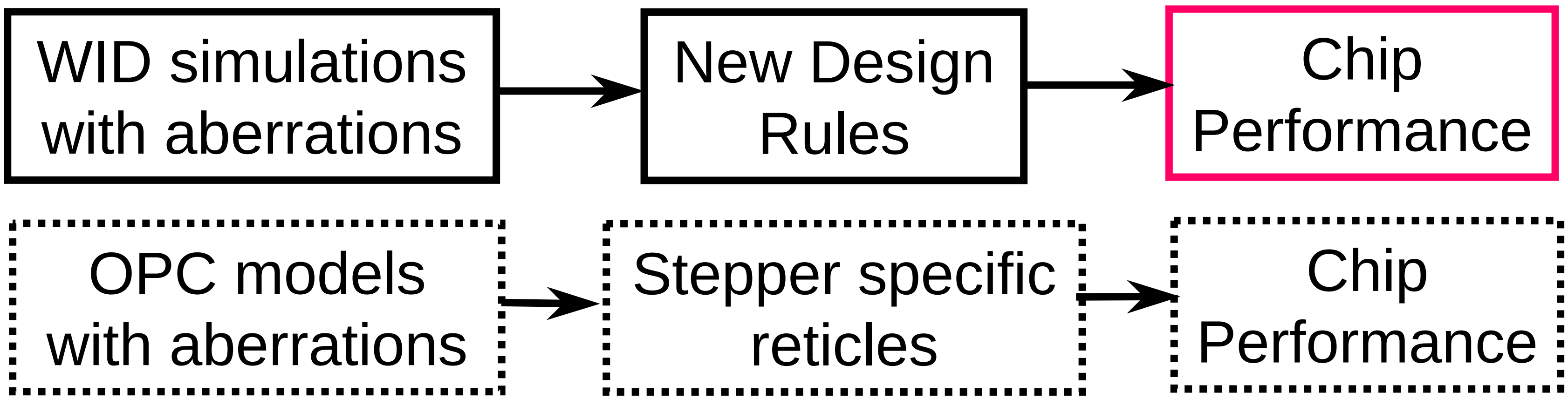
Hierarchy of resist models: leverage physical models to build/strengthen OPC models



Example 2: stepper aberrations

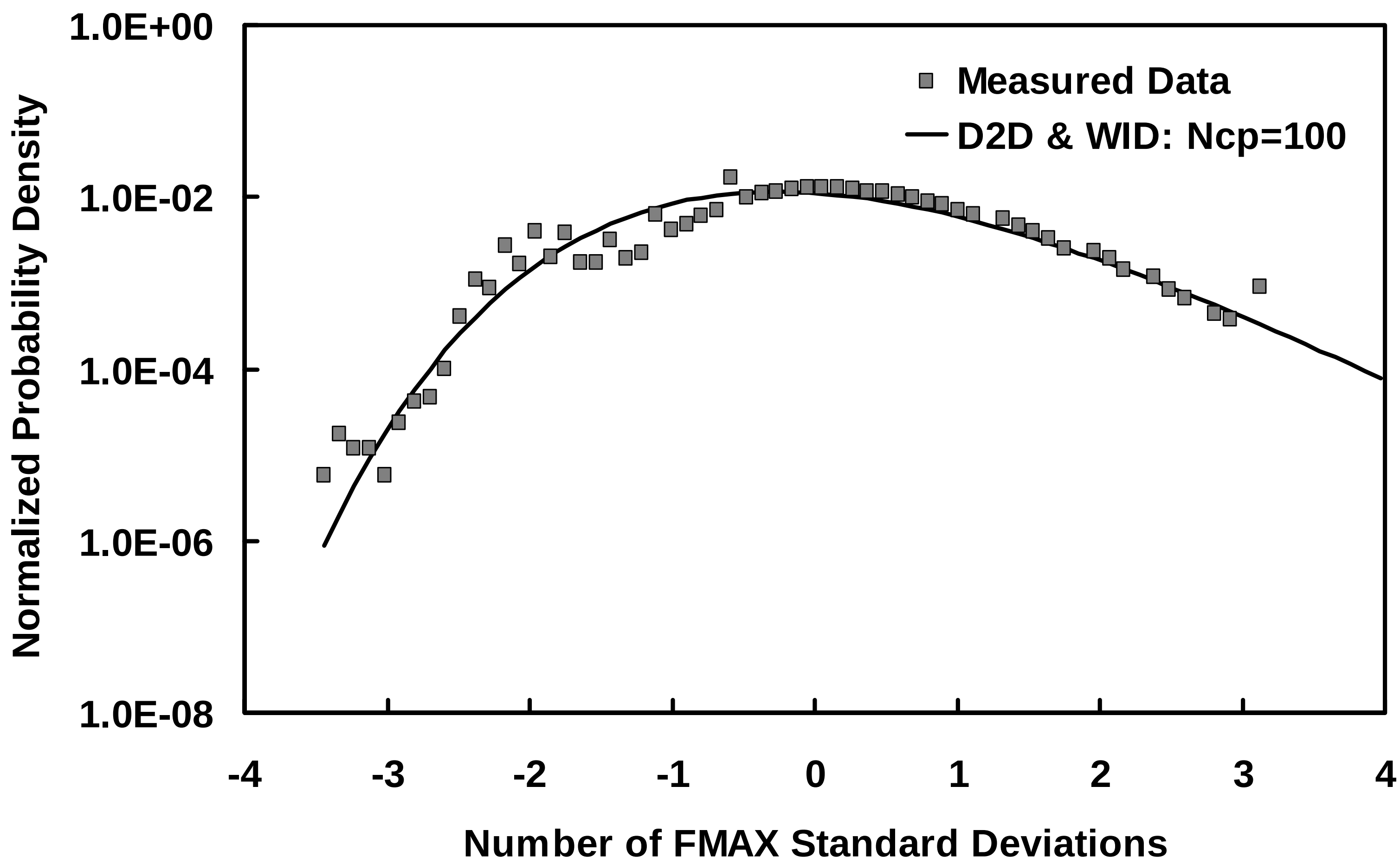
- Stepper aberrations are the most common example of systematic aberrations, and several routes are possible for accomodating this effect in design

- Measurement of aberrations has become a credible, if not routine, operation



- Also, as before, we can minimize aberrations. Focus here on why it is more desirable to minimize systematic (rather than random) variations.

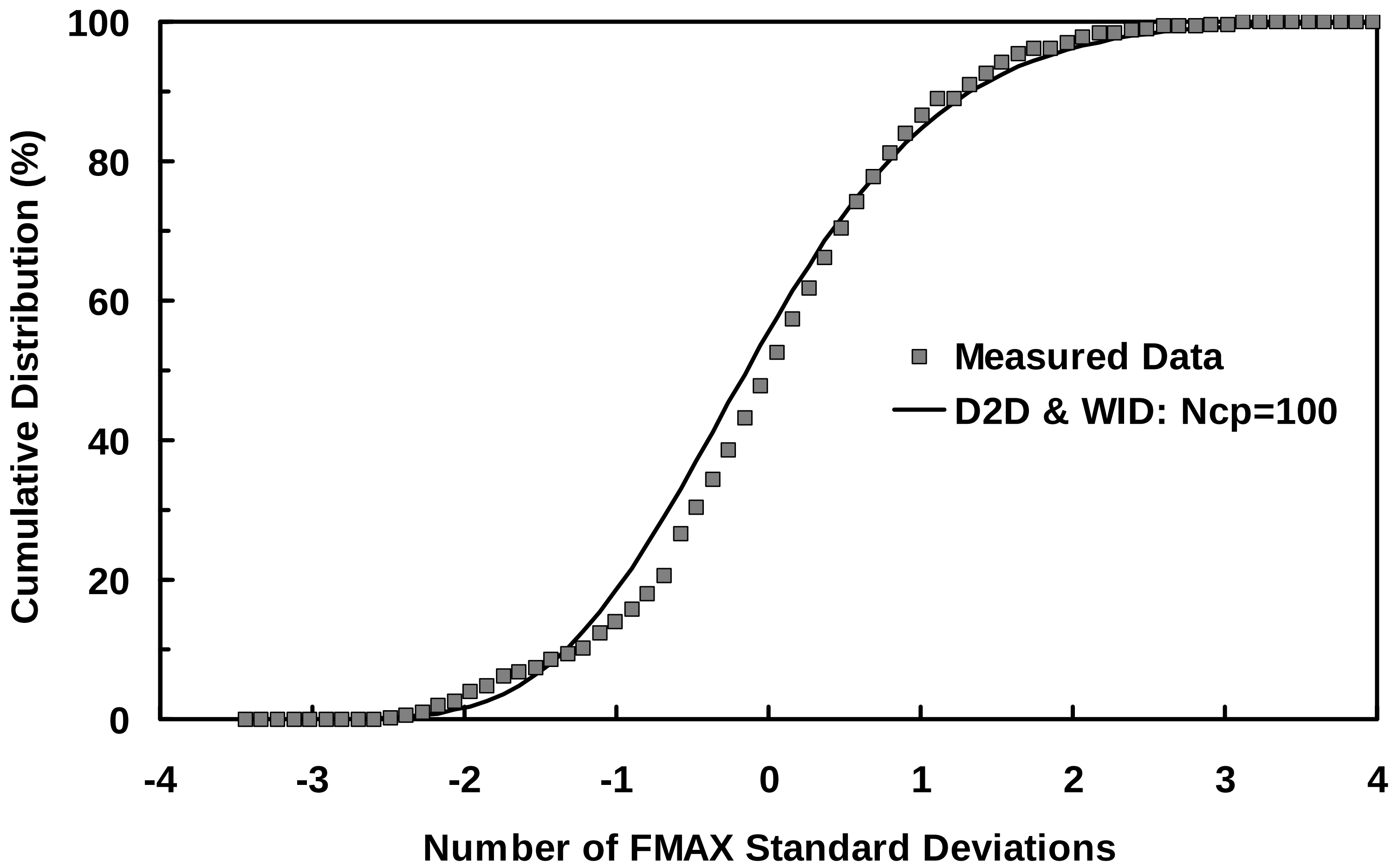
FMAX Probability Density



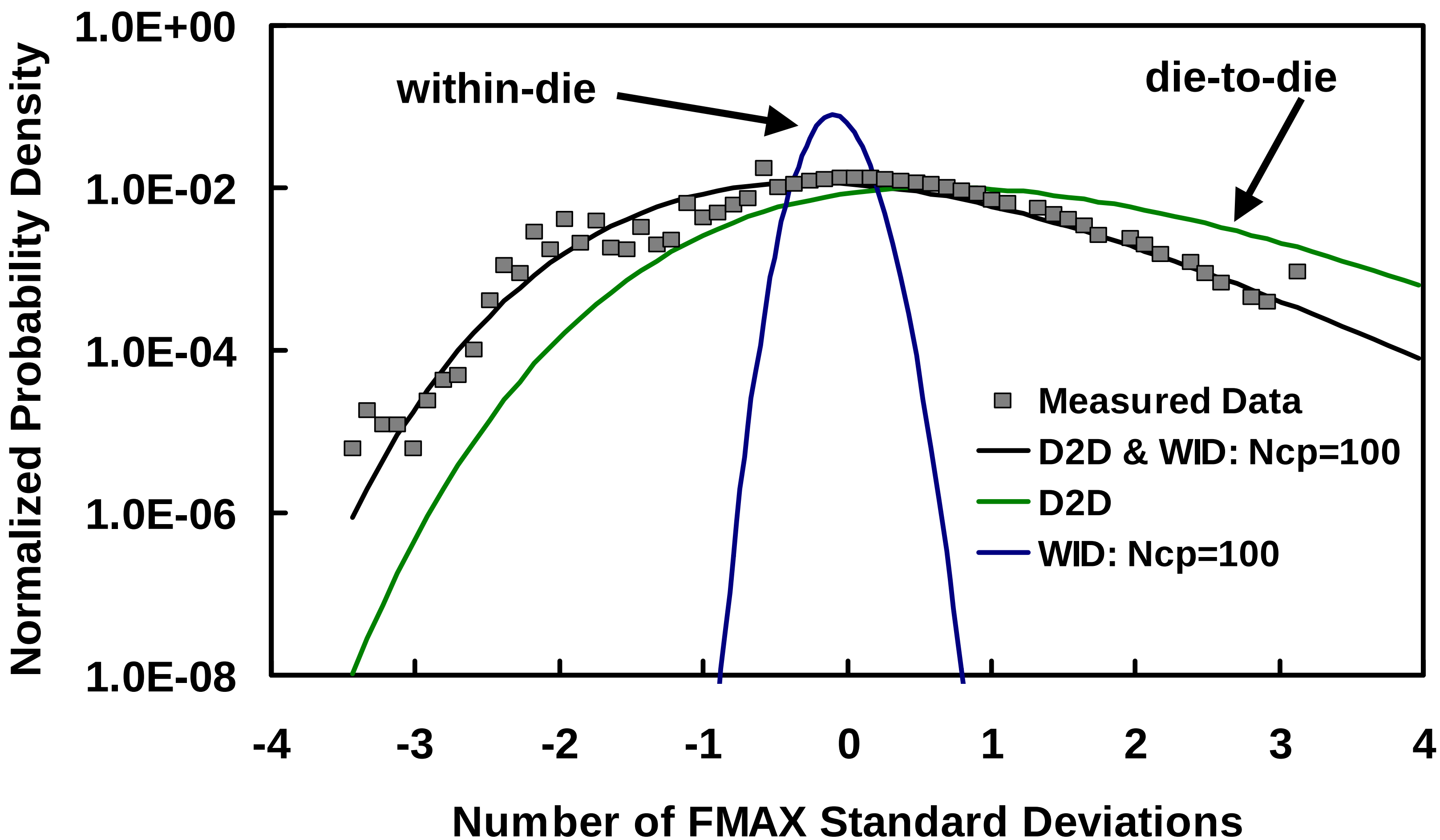
- **Model agrees closely with measured data for a recent 0.25 μm microprocessor in *mean*, *variance* and *shape***

Bowman, Duvall, Meindl, IEEE J. of Sol. State Circuits, 2002

FMAX Cumulative



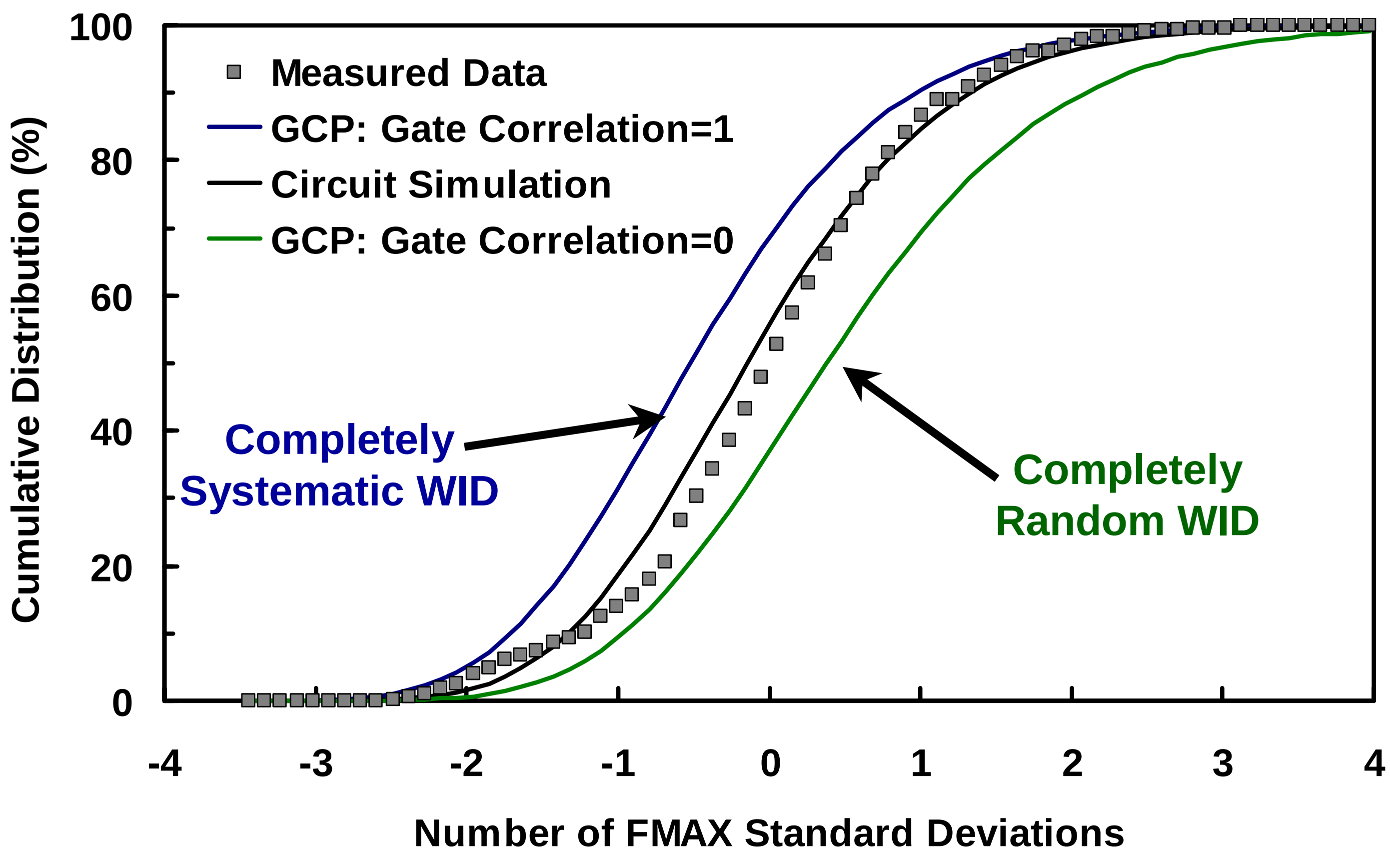
Individual Contributions of Die-to-Die and Within-Die Fluctuations



① ***Within-die fluctuations impact the FMAX mean***

② ***Die-to-die fluctuations impact the FMAX variance***

Systematic vs. Random

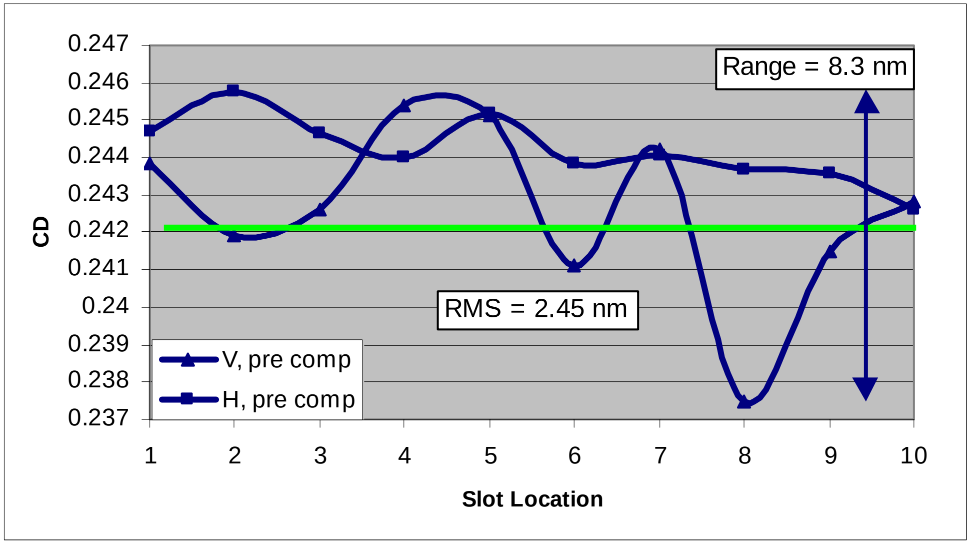


- ***Systematic within-die fluctuations*** **decrease the FMAX mean more severely than** ***random within-die fluctuations***

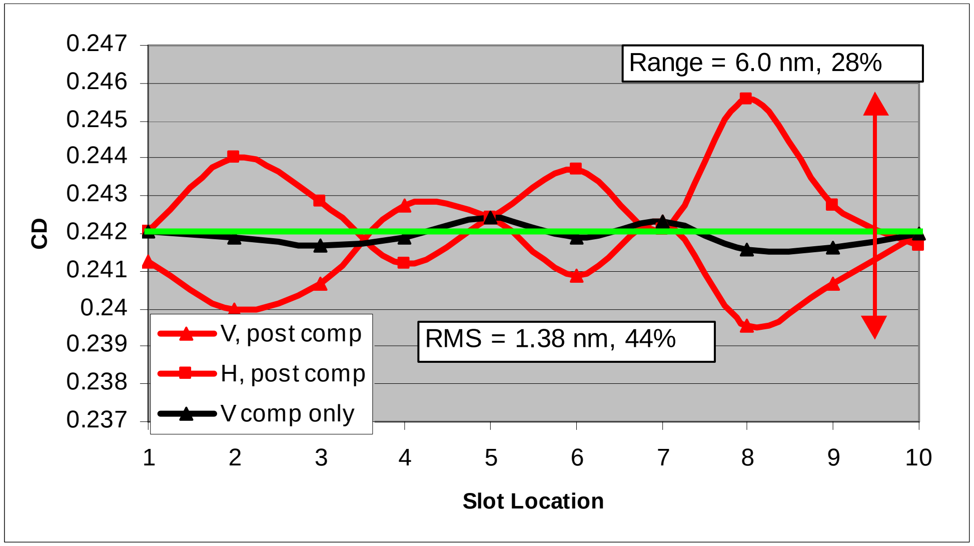
<u>Conclusion</u>: It pays to reduce aberrations, more than, say, LER.

Example of minimizing impact of systematic variations: Across slot dose compensation

before

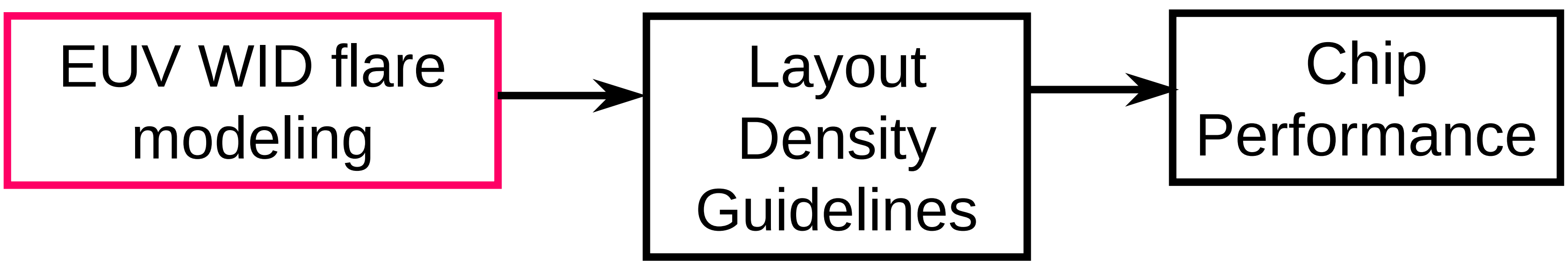


after



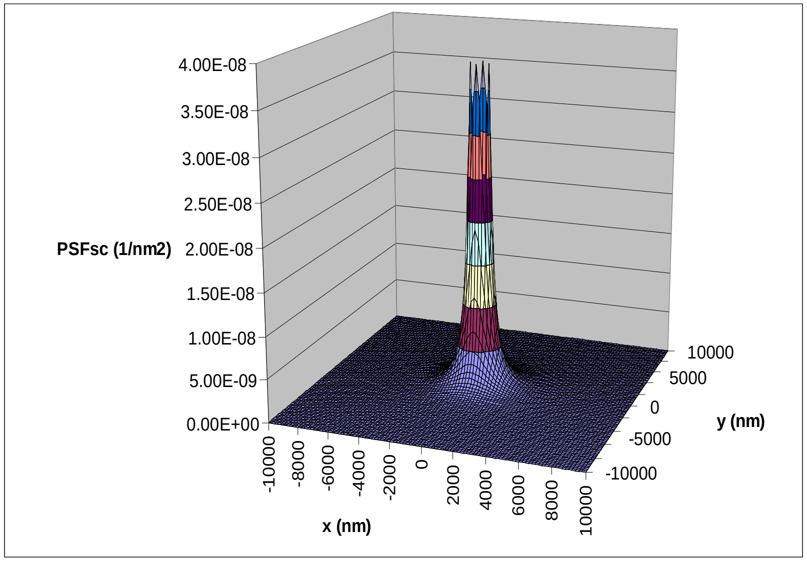
Example 3: Layout dependent flare in EUV

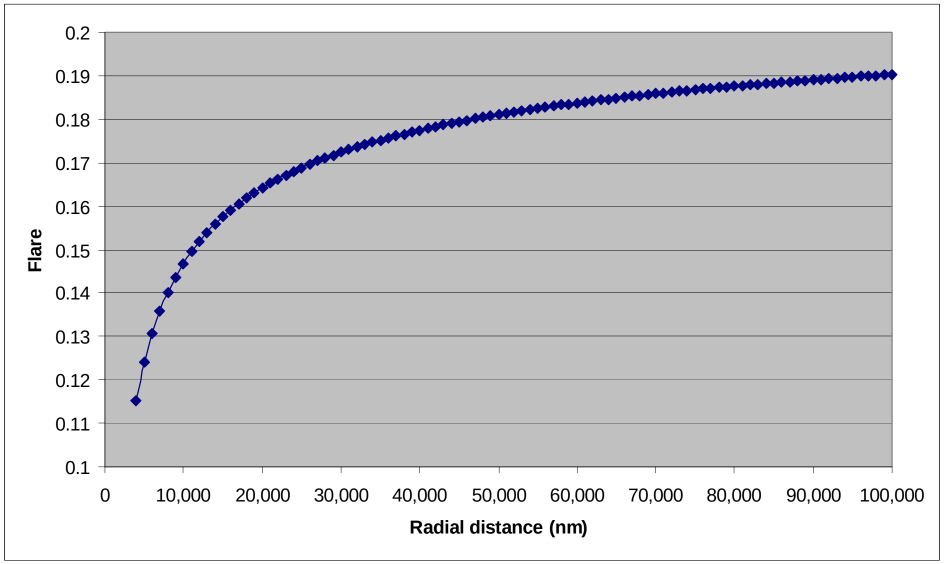
- Rough mirrors in EUV optics cause scattering, or flare.
- Flare and flare variation causes WID CD variation.
- “Long range” layout variations affect local flare.
- Layout can be modified to minimize such flare variation.



PSF due to scattering

$$\mathrm{PSF} = \frac{0.166}{r^{2.39}} \frac{1}{\mathrm{nm}^2} \quad \text{for } r > 600\mathrm{nm}, \text{ zero otherwise}$$





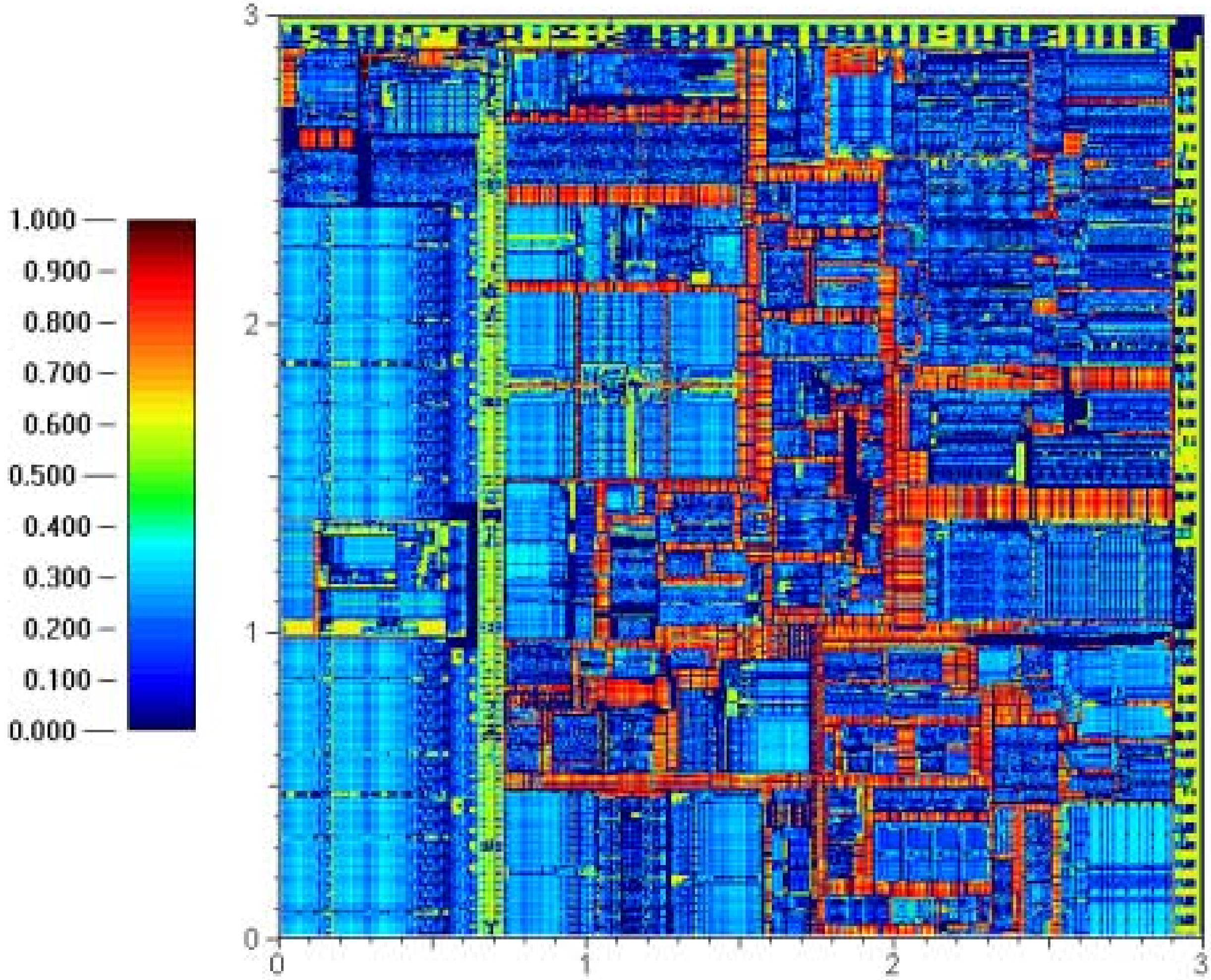
After a sharp fall, PSF decays very slowly

As a result, “far away” layout geometry affects local flare

PSF courtesy J. Bjorkholm

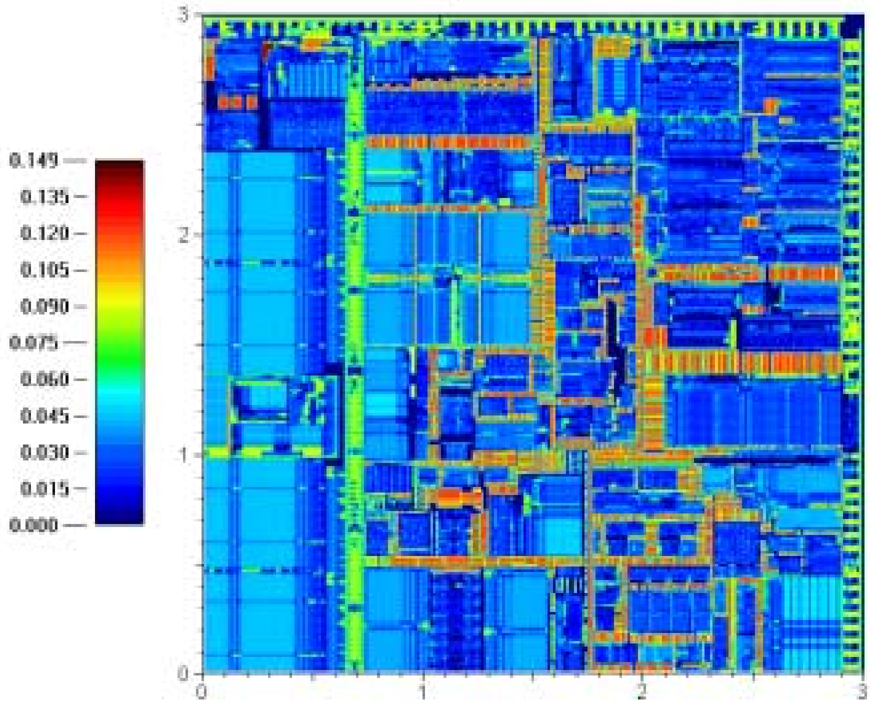
3mm x 3mm piece of estimated layout for EUV technology

- Layout density is extracted on a 1um grid
- Due to large scale effects, need to perform calculation on large area – in this example, the convolution is 95% accurate in the middle.

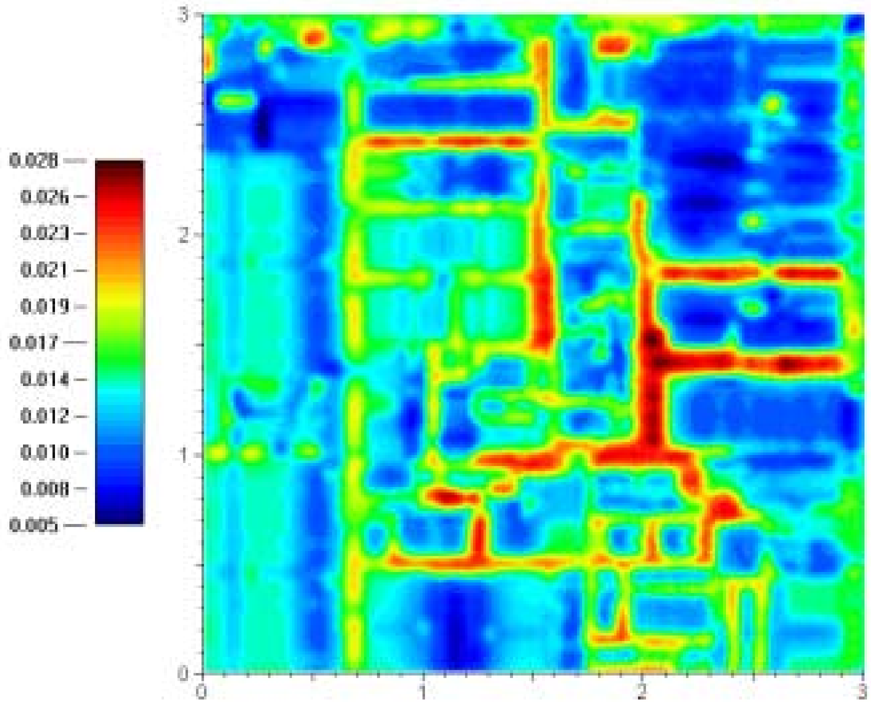


Maps courtesy N. Gupta

Components of flare contributions

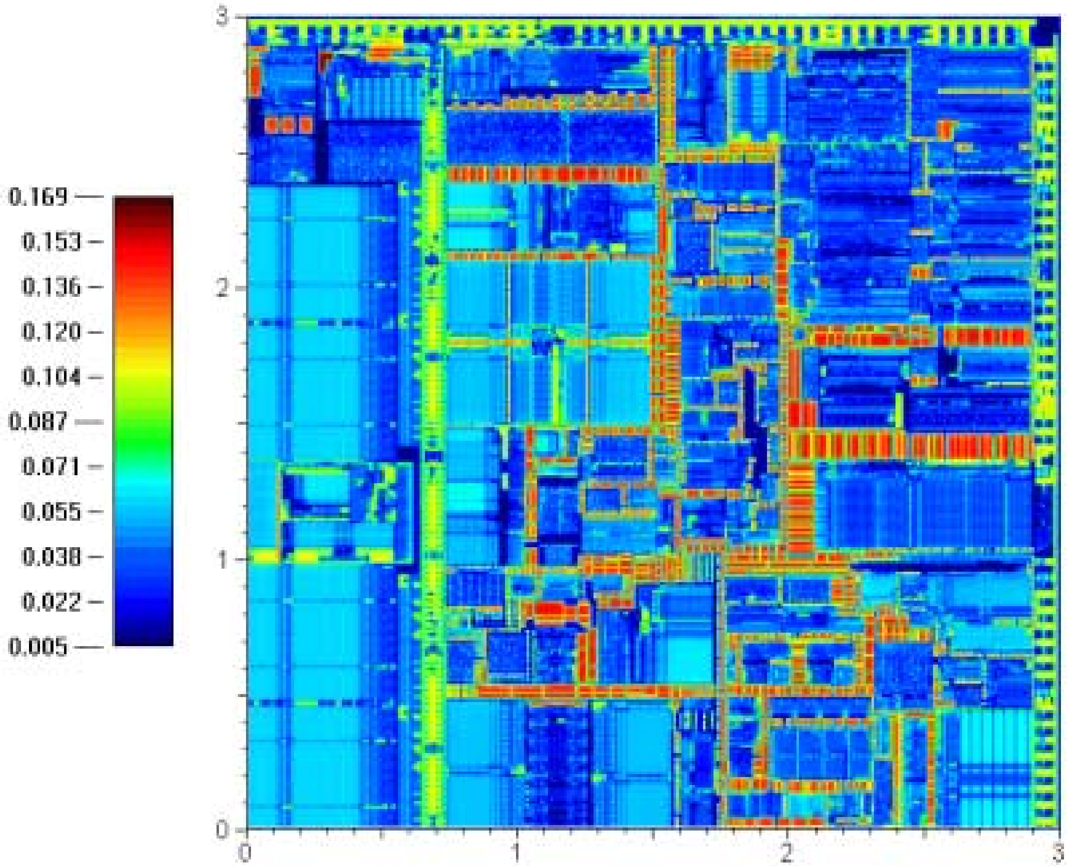


Short range (μm)
component



Long range (mm)
component

Final flare result for (3mm)^2 patch

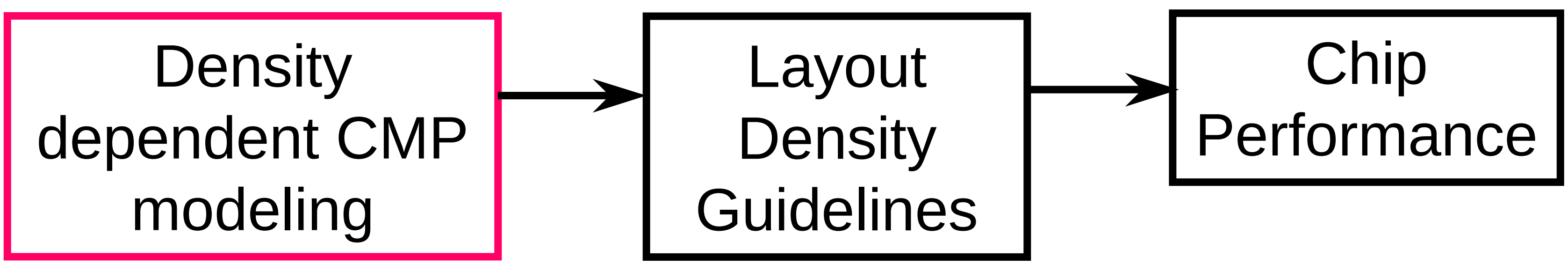


Max = 16.9%
Min = 0.54%
Rng = 16.4%
Avg = 5.62%

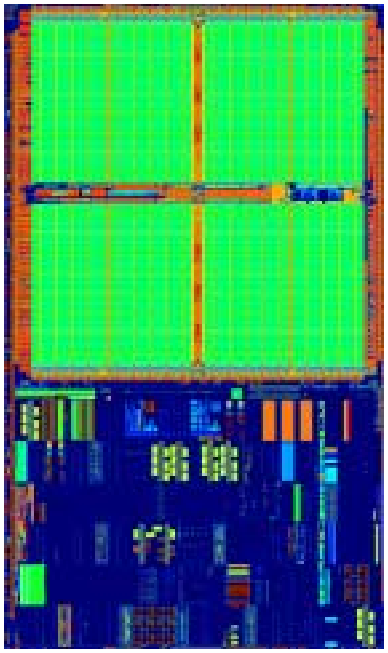
Conclusion: Placing dummy features on layout can significantly reduce layout density variation, thereby reducing WID variation due to flare.

Example 4: Layout dependent CMP

- Polish rate is affected by density of features.
- Controlling density variations leads to better post-polished thickness uniformity.
- Thickness uniformity affects subsequent CD variations.
- Dummy features can be added to control density variations.

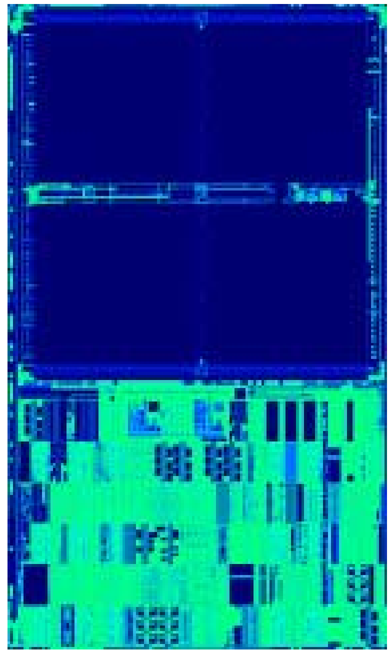


Optimal dummy density simulations



device only density map

+



dummy only density map

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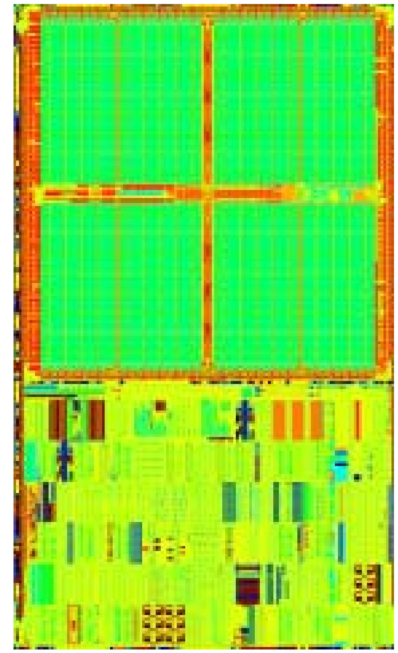

Device + dummy density map

Dummy density varied from 30% - 60%

Pitch (dummy width + space) varied from 0.6um - 1.2 um.

Future directions

- Ideally speaking – further integration of different models and simulators should allow development of more process aware designs
- BUT….stiching two models togethers runs the risk of convolving the errors in each one
- Several exciting paths exist beyond the relatively simple modifications to design described here
  - Inclusion of OPC as a true RET option when evaluating future lithography options
  - Coupling between physical layout and electrical simulations

Conclusions

- For high performance chips, process variation has to be low – this can be done by
  - Minimizing the cause of the variation
  - Adjusting the design to accommodate residual variations
- TCAD can provide both physical models and a comprehensive infrastructure to serve as a bridge between process and design
- Several examples from Lithography and CMP demonstrate the application of TCAD to create process aware designs